

ABSTRACT OF THE DISCLOSURE

5      A serial bit transparent data transferring technique  
eliminating the bit ambiguity problem of the standard time-  
division multiplexing/demultiplexing architecture without  
introduction of any extra latency. A serializer multiplexer  
converts input parallel data words into a serial data bit  
10      stream under control of a serializer timing circuit. An output  
multilevel buffer retimes the serialized data and increases  
the amplitude of certain bits with a preselected value to mark  
positions of out-going serial data words. The bits are defined  
by a serializer digital data converter also controlled by the  
15      same timing circuit. The imposed marking pulses are retrieved  
from the input serial data stream by a multilevel input  
detector of a deserializer timing circuit and used for the  
synchronization of the demultiplexing operation. As a result,  
20      the deserializer directly reconstructs the original bit order  
from the serial data bit stream with no extra bits, thus  
providing minimal possible latency and full data rate.